Craig Mautner

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PROGRAMMING LANGUAGES

Fluent: C, C++, PERL, UNIX shell scripts, Assembly (MIPS, ARM, 68K, 8051, DSP, 68xx, PIC, 8260 CP, C5).
Experience in: Java, Python, Matlab, TCL/Tk, Fortran, Pascal, ml, sml, FORTH, BASIC, LISP.

TOOLS

In Circuit Emulator, Logic Analyzer, Oscilloscope, Spectrum Analyzer, compilers, linkers, assemblers, debuggers, FPGA development tools: Xilinx, Altera. Microsoft Office including Project, VISIO.

OPERATING SYSTEMS AND ENVIRONMENTS

Linux, RTOS (VxWorks, pSOS, VRTX, AMX), Windows, UNIX

EMPLOYMENT AND TECHNICAL EXPERIENCE

COASTAL SENIOR CONSULTING, INC. 1/02 – Present

President. Contractor for embedded systems programming. Clients and projects include:

Pioneer Digital Technology. Cable TV set top box (dual tuner, High Definition, Digital Video Recorder):

* Porting of PowerTV OS onto Linux.
* Implemented dual-stream Digital Video Recorder (generating two patent applications for Pioneer).
* Integrated Conditional Access (Scientfic Atlanta's PowerKEY).
* Wrote Linux device drivers for Digital Video Recorder, Smart Card, MPEG Transport.
* C and C++ coding of application and middleware (PowerTV) level software.

Vision Robotics, Inc. Wrote software for robotic vacuum cleaner:

* Utility algorithms for room mapping.
* Physics model of motion for camera simulator.
* Room simulator using OpenGL and VRML.
* Vacuum hose simulator in octave (open-source version of matlab).

WINDRIVER, DOCTOR DESIGN SERVICES 9/92 – 1/02

Project Manager, Senior Member Technical Staff. Responsible for design and development of embedded computer and electronic systems. Tasks include: software and hardware implementation and debug; software and hardware architecture; design reviews, system specification; customer and vendor interface; proposal writing; formation and management of project teams.

Individual projects include:

* Microcoding and C code of Network Address Port Translation algorithm to C-5 Network Processor.
* Architecture design and port of WindRiver's Digital Media Framework, multimedia middleware library, to Teralogic Cougar Set Top Box (WindRiver).
* Architecture study of a satellite controlled laptop security device for disabling and recovery of stolen laptops (CyberGroup Networks).
* Microcode written for Motorola 8260 Communications Processor to assemble and route packets below the PowerPC level in a cell phone base station. Included writing a debugger in TCL/Tk (Motorola).

* Architecture design and coding of Bluetooth and GPRS enabled Personal Digital Assistant (Xircom).
* Porting of JAVA KVM graphics engine to WindRiver's WindML graphic library (WindRiver).
* Architecture design and software specification for integration of TiVo consumer hard disk recording system with DirecTV satellite reception (TIVO).
* Addition of Dolby AC-3 reception to existing DirecTV Set Top Box (SONY).
* Set Top Box Software - Managed team of 10 engineers responsible for writing the software for Pioneer's next generation analog Set Top Box. Device is capable of displaying program guides, ordering Pay Per View programs, executing downloaded applets. Additional responsibilities included User Interface design.
* Cable Headend Transmitter - Managed team designing a rack-mounted device to receive messages over ethernet and retransmit them over an RF cable-TV path. Additional responsiblities included mechanical packaging (Pioneer).
* Internet Terminal - Managed team designing a home internet device for web-surfing from a couch (Philips).
* Set Top Box Cost Reduction - Managed team responsible for redesigning the hardware of Set Top Box in order to reduce the overall cost. 25% cost savings achieved (SONY).
* Set Top Box Software - Managed team of 15 engineers responsible for writing the software for SONY's DirecTV Set Top Box. (SONY)
* Fingerprint Matching System - Cost reduction and performance enhancement of existing Automatic Fingerprint Identification System. Rearchitected seven 11"x11" boards into two PC-EISA form-factor boards. Resulting system composed of Am29200 RISC processor, three 320C50 DSPs, and eight Xilinx FPGAs. Additional responsibilities included design of two FPGAs, programming the Am29200 and the DSPs (Printrak).
* Debugger Platform - An In Circuit Emulator for developing Nintendo and Sega based games. Debugging capabilities included hardware breakpoints and software trace. Project included packaging, board design, and FPGA design (Leland/Williams).
* DirecTV Bitstream Capture Generator System - Managed team responsible for design and programming of Satellite signal logic analyzer and emulator. System consisted of PCI board in a PC transferring satellite data between PC and Set Top Box (SONY).
* Wireless Cable Headend and Downconverter - Managed team responsible for design of a Wireless Cable (Microwave transmission) transmission and reception system. Design included MC68340, NTSC encoder, PIC16C65 and two custom FPGAs, DES Encryption/ Decryption. Additional responsibilities included PIC programming and package design (Pacific Monolithics),
* Medical Imaging Terminal - Repackaged a 16" portrait mode LAN based x-ray and CAT-scan viewer into a 21" system (Genesys).
* Design review analysis and repair of fiber optic SCSI extender. Turned customer's unreliable product into a highly reliable one (AppliedConcepts).
* Two Field Programmable Gate Array designs to enable prototype and debug of Demodulation and In Band Signaling for a satellite delivery system (Comstream).
* SCSI Adapter Board - Managed quick turn fabrication and testing of adapter boards for a COMPAQ Lite notebook PC (Mitchell).
* Network Backup System - Managed and designed network hardware backup system. Design of RS-232 controlled SCSI switch and dual redundant power supply switch. Packaging of system. Patent pending for this design (NetGuard).
* Clock Chip Feasibility Study - Analyzed market and features for a Clock Chip for Set Top Box (Pericom).

UC SAN DIEGO, COMPUTER SCIENCE AND ENGINEERING 9/88 - 8/90; 9/97 - 5/00

Graduate Student/Fellow. Research in Evolutionary Robotics: using evolutionary algorithms to discover body plans and neural network control structures for robots (see publications below). Master's project was a study of transitions to Chaos in Cellular Automata Rule Space. Coursework included Computer Architecture, Compilers, Operating Systems, Algorithms and Data Structures, Software Engineering, Imperative and Functional Programming Languages, Complexity Theory, Artificial Intelligence, Neural Networks, and Cognitive Science. GPA 4.0+. Withdrew from program prior to completion of Ph.D.

DATA/WARE DEVELOPMENT 9/90 - 9/92

Director of Engineering. Responsible for directing the efforts of Engineering (design, test and manufacturing

groups), Drafting, and Document Control departments. Data/Ware's product line consists of optical storage for mainframe computers as well as test equipment for parallel and fiber optic mainframe I/O channels. Responsibilities included personnel decisions, product planning, technical direction of staff, scheduling and tracking projects, yearly budget, mediating and resolving issues between and within departments.

10/85 - 9/88

Product Development Engineer. Designed several software and hardware products culminating in a mainframe attached optical storage system. All projects involved emulation of mainframe I/O channel or of channel attached peripherals. Responsible for specifications, architecture, prototype, programming, debugging and transfer to manufacturing. Supervision of team of four to six engineers throughout optical project. Product became largest selling direct mainframe attached optical storage system worldwide.

8/83 - 1/85

Project Manager. Responsible for taking project from initial hardware and software design through to production. Managed other engineers, programmers, and technicians. Participated in customer service and marketing effort. Management duties included supervising engineers and technicians, scheduling, writing progress reports, organizing test procedures, and working closely with production, purchasing and marketing departments.

TELEDYNE CONTROLS 2/85 - 10/85

Design Engineer. Designed, built and tested Floating Point Co-Processor for 68000 based single board computer. Design utilized bit-slice architecture and a dedicated floating point chip-set. Designed assembly language for definition of 80 bit wide microword required by hardware. Programmed completed system to perform real time Fourier analysis using floating point exponentiation, sine, and cosine functions as well as addition, subtraction, multiplication and division. Wrote documentation for entire system, including: hardware, firmware, and single board computer software interface.

SCRIPPS INSTITUTE OF OCEANOGRAPHY,
INSTITUTE OF GEOPHYSICS AND PLANETARY PHYSICS 9/81 - 8/83

Jr. Development Engineer. Began work as a student technician fabricating electronics for geophysical instrumentation, later promoted to Engineer. Duties included design of analog circuits for signal conditioning and processing. Design of digital circuits for calibration and support equipment. Maintained and repaired geophysical instruments at remote field station/observatory. Instruments include long baseline laser interferometer, fluid tiltmeter, and seismometers. Design and construction of support equipment for absolute gravity meter. Ordering parts and materials for projects at lab and observatory. Routine metal work on drill press, sheet metal tools, lathe and mill. mechanical drawings for fabrication of small parts.

EDUCATION

* Candidate in Philosophy (A.B.D.) - Computer Science and Engineering, UC San Diego, 1999
* Master of Science - Computer Science and Engineering, UC San Diego, 1988-90
* Bachelor of Science - Physics, UC San Diego, 1977-83. Minors in Electrical Engineering and Mathematics

AWARDS AND HONORS

* Patent # 5,455,926 October 3, 1995 VIRTUAL ADDRESSING OF OPTICAL STORAGE MEDIA AS MAGNETIC TAPE EQUIVALENTS
* Patent #5,438,674 Aug 1, 1995. OPTICAL DISK SYSTEM EMULATING MAGNETIC TAPE UNITS.
* UCSD Research Review award for best poster in CSE department, Feb 2000
* National Science Foundation Fellowship, 1989/90.
* Powell Foundation Fellowship, 1988/89.
* UCSD CSE Department Award of Distinction (Spring 1990) for highest score on department Comprehensive exams.
* Graduated Cum Laude, UCSD 1983.
* UCSD Provost's Honors 1977-1983.
* National Merit Scholarship finalist, 1977.

PUBLICATIONS

Craig Mautner and Richard K. Belew. Evolving Robotic Bauplans. In 5th Joint Symposium on Neural Computation, page 93, University of California, San Diego, 1998. Institute for Neural Computation.

Craig Mautner & Richard K. Belew. Evolving Robot Morphology and Control. Proceedings of the Artificial Life and Robotics Conference (AROB99).

Craig Mautner & Richard K. Belew. Coupling Morphology and Control in a Simulated Robot. in Proceedings of the Genetic and Evolutionary Computation Conference (GECCO) 1999.

Craig Mautner & Richard K. Belew. Testing Simulated Controllers in Real Robots. GECCO 99 Birds-of-a-feather Workshop on Evolution of sensors in nature, hardware and simulation.